DETAILED ACTION

1. As per the instant Application having Application number 10/814,968, the examiner acknowledges the applicant's submission of the amendment dated March 19, 2008. At this point, claim 1 has been amended, and claims 4, 13-14, 16-20 and 22 were previously cancelled. Claims 1-3, 5-12, 15 and 21 are pending.

REASONS FOR ALLOWANCE

2. The following is an examiner's statement of reasons for allowance:

3. The subject matter of claims 1-3, 5-12, 15 and 21 is considered as allowable subject matter.

4. The primary reasons for allowance of claim 1 in the instant application is the combination with the inclusion in these claims of the limitation of method/system for simultaneously performing a write operation and a read operation wherein "**when the write address and the read address are the same as a data memory address, the read operation, is performed in the data memory block and the write operation is performed in the sub-memory block, and wherein when the write address and the read address are both not the same as the data memory address, the operation corresponding to the address that is the same as the data memory address is performed in the data memory block and the operation corresponding to the address that is not the same as the data memory address is performed in the sub-memory block**." The prior art of record neither anticipates nor renders obvious the above recited combination.

5. The primary reasons for allowance of claim 12 in the instant application is the combination with the inclusion in these claims of the limitation of method/system for simultaneously performing a write operation and a read operation wherein "**determining if an upper address of the write address is the same as an upper address of the read address, when the write address and the read address have been input during the period of the clock signal; and performing a write operation and a read operation such that upon determining that the write address and the read address are the same as a data memory address, the read operation is performed in the data memory block and the write operation is performed in the sub-memory block and upon determining that the write address and the read address are both not the same as the data memory address the operation corresponding to the address that is the same as the data memory address is performed in the data memory block and the operation corresponding to the address that is not the same as the data memory address is performed in the sub-memory block**." The prior art of record neither anticipates nor renders obvious the above recited combination.

6. The primary reasons for allowance of claim 21 in the instant application is the combination with the inclusion in these claims of the limitation of an integrated circuit for simultaneously performing a write operation and a read operation wherein "**a tag memory controlling unit, which writes data to the memory blocks or reads data from the memory blocks in response to the write address or the read address, wherein access to the same sub-memory block is not simultaneously performed when the write address and the read address are the same, wherein the tag memory controlling unit has a same number of decoding addresses as a number of addresses**

for decoding the data memory blocks and a number of columns and rows different from a number of columns and rows of the data memory blocks." The prior art of record neither anticipates nor renders obvious the above recited combination.

7. Dependent **claims 2-3, 5-11 and 15** are allowable at least for the reasons recited above as including all of the limitations of the allowable independent base claims upon which they depend.

8. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

DIRECTION OF FUTURE CORRESPONDENCES

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571)272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

IMPORTANT NOTE

10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571)272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

April 7, 2008

/Yaima Campos/
Examiner, Art Unit 2185

/Sanjiv Shah/

Supervisory Patent Examiner, Art Unit 2185